

Recruitment information: A Researcher
for Department of Electronics, Graduate School of Engineering
Nagoya University, Japan

1. Affiliation

Nagoya University, Faculty of Engineering Building No.3
(Higashiyama Campus : 1 Furo-cho, Chikusa-ku, Nagoya, Aichi, Japan)

2. Number of Positions

One researcher

3. Expected Starting Date

Earliest Possible date After October 1st,2019

4. Research Outline

Research on superconducting quantum circuits (quantum bits) and superconducting logic circuits to control and readout their quantum states. The project is particularly aimed at a realization of scalable superconducting quantum circuits and low-consumption-power superconducting logic circuits by implementing ferromagnetic Josephson junctions as well as their monolithic integration.

5. Research Themes

To realize the novel superconducting quantum circuits with the ferromagnetic Josephson junction, the research themes are as follows:

- 1) Development of the implementation and measurement setup based on a dilution refrigerator system for the superconducting quantum circuits.
- 2) Fabrication, characterization, and analysis of the superconducting quantum circuits.

6. Qualifications

A person with a doctorate or a person who expects to obtain a doctorate by the time of arrival.

7. Recruitment fields

- 1) Superconducting electronics.

Applicants who are motivated to work on the superconducting quantum circuits with following backgrounds are also favorable:

- 2) Low temperature physics experiments by using dilution refrigerators etc.
- 3) Analog integrated circuits

8. Period of Employment

1 year until March 31,2020 and employment renewal every year.

9. Working Condition

Discretionary labor system

Holiday: Saturdays, Sundays, national holidays, New Year's holidays (December 29-January 3)

Vacation: Annual paid vacation (6 months after employment), summer vacation (university designated date)

Subscription Insurance: health insurance, welfare pension, employment insurance, worker's compensation insurance

10. Salary Salary will depend on quantifications experience, based on Nagoya University's Rules for Employees to whom the Annual Salary System applies.
11. Selection method
 After screening for documents, we conduct interviews and decide on the acceptance.
12. Application Documents
 Send a set of the following items by mail to the address below with a note "Application to researcher for department of electronics, graduate school of engineering Nagoya University" written in red on the front of the envelope together with sending pdf file of the following items by e-mail. Or an USB memory stick with a set of above information included as a pdf file.
- (1) Curriculum vitae with face photograph and e-mail address
 - (2) List of publications (Original referred articles, International conference proceedings, Reviews, Books, Patents, Awards, Invited lectures, etc.)
 - (3) Reprints of three representative publications
 - (4) Other items the applicant considers useful for selection (education experiences, social activities, etc.)
 - (5) A list of acquired research funds
 - (6) Research plan and essay on applicant's policy on education (about 1-2 pages)
 - (7) Name, affiliation, and e-mail address of one contact references
13. Deadline
 August 20, 2019 (Deadline for receipt)
 As soon as the candidate is confirmed application is closed.
14. Enquiry about the position
 Prof. Taro Yamashita
 Department of Electronics, Graduate School of Engineering, Nagoya University,
 1 Furo-cho, Chikusa-ku, Nagoya, Aichi, 464-8603, Japan
 Phone: +81-52-789-3158 (secretary)
 E-mail: yamashita@nuee.nagoya-u.ac.jp
15. Personal information submitted in connection with this public offering shall be used only for the purpose of selection and, after completion of selection, all personal information will be discarded responsibly, except for the information of those who have passed the selection.